# newelectronics

23 October 2018

**MEDICAL ELECTRONICS • ELECTRONICA 2018 PREVIEW • EMDEDDED DESIGN** 







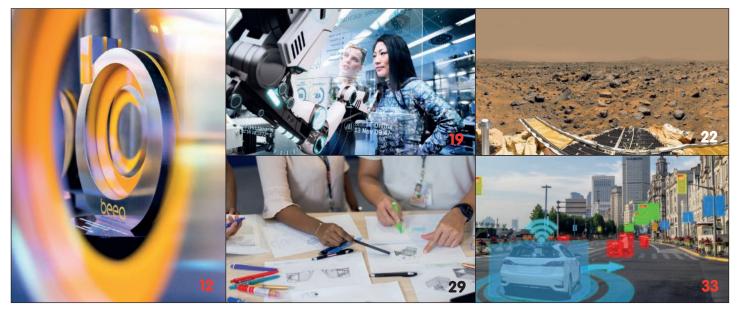
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Cover Photography: Karla Gowlett

#### COMMENT

Compared to an ailing steel industry, just a few years ago, the semiconductor industry is now witnessing a boom

#### **NEWS**

Qualcomm to extend the Wi-Fi experience with a new chipset of 60GHz 802.11ay solutions

A new technique developed by scientists at MIT means that expensive silicon wafers can now be repliicated

Research team uncovers serious security gaps in 5G mobile communications standard

Last month saw the launch of a 5G test bed in Brighton, showcasing the latest innovation and technology 10

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#### Bridging the gap to the future

This year's BEEAs saw AESSEAL win the Grand Prix prize for its outreach engineering programme and its long-term engagement with the wider community. By Neil Tyler

#### **DESIGN PLUS**

#### Reinventing 'flat' education

So far schooling has relied on 2D screens and textbooks. An AR/VR laptop could revolutionise the way students are taught, according to Bethan Grylls

#### **ELECTRONICA 2018 PREVIEW**

#### Just connect

As exhibitors and visitors prepare for electronica 2018, how has the event evolved over the years and what can visitors expect at this year's show? Bethan Grylls reports

#### **EMBEDDED DESIGN**

#### **Loose threads**

As IoT and distributed cyber-physical systems become more sophisticated, timing is proving increasingly challenging, as Chris Edwards explains

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According to Arm, without safety there is no future for autonomous driving, as Neil Tyler discovered

#### **MISSION STATEMENT**

'New Electronics keeps designers and managers abreast of the latest developments in the world's fastest moving industry'



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## Semiconductor boom

COMPARED TO AN AILING STEEL INDUSTRY, JUST A FEW YEARS AGO, THE SEMICONDUCTOR INDUSTRY IS NOW ENJOYING BOOMING CONDITIONS



ccording to Wally Rhines, the President and CEO of Mentor, we are seeing a wave of very strong growth in the semiconductor industry. Last year it grew by 22 percent and not all of that came from memory – in fact non-memory markets were ahead by over 8 per cent, way up on recent years.

Just a few years ago the industry was described as mature and over-burdened with infrastructure, and was compared to the struggling steel industry. In fact, the design of semiconductors had become so expensive that very few new businesses were able to enter the market.

Fast forward a year, and we are now seeing a wave of growth with hundreds of new entrants coming into the market. Crucially, money is now available for investment, particularly for companies developing new application specific processors that deliver a specific type of functionality, which means that the processor can be optimised.

According to Rhines, design activity, research and development and, significantly, risk takers have returned to the market. Venture capital spending in fabless semiconductor production has skyrocketed over the past year and could touch \$2billion in 2018. Just a few years ago that figure was running at just \$300million.

So what's driving this new wave of growth? Well, there are more companies looking to design their own chips for one thing. Bosch is building its own fab, for example, while Tesla is looking to develop its own chips.

The cost of development has tumbled too. New tools are making it possible to develop chips and the use of high level synthesis is cutting not only the cost, but also development times. By using high level synthesis techniques, as opposed to traditional methods, it's possible to deliver a product in a quarter of the time.

At the end of the day though, the biggest driver appears to be growth in China. Both at corporate and state level the investment being made in semiconductor research and development, as well as manufacturing, is massive. The Chinese government is investing \$20billion in the industry each year, and that is being matched by private investors. And further significant investment is being rumoured.

According to Rhines, China has invested six times that of the US in the past few years and that's a trend that's expected to accelerate.

The world is changing and China's investment binge could pose a real threat to the on-going dominance of the US – but wherever that growth is coming from, the EDA industry looks set fair for a productive and very profitable few years.

Neil Tyler, Editor (neil.tyler@markallengroup.com)

"The world is changing and China's investment binge could pose a real threat to the on-going dominance of the US."











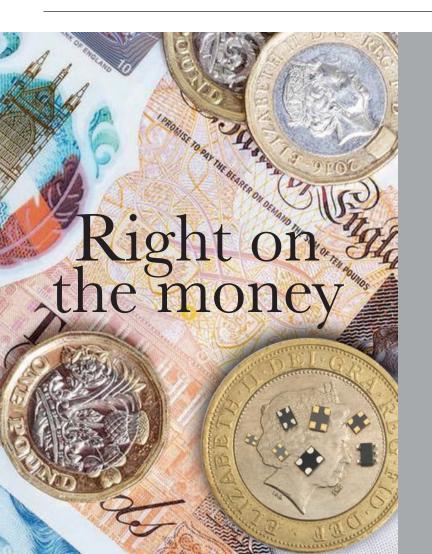
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#### ISSN 0047-9624 Online ISSN 2049-2316

Annual subscription (22 issues): UK £108. Overseas; £163. Airmail; £199. New Electronics, incorporating Electronic Equipment News and Electronics News, is published twice monthly by MA Business, Hawley Mill, Hawley Road, Dartford, DA2 7TJ. T: 01322 221144 E: ne@markallengroup.com

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## newelectronics Next generation Wi-Fi chipsets

QUALCOMM EXTEND WI-FI EXPERIENCES WITH 60GHZ 802.11AY SOLUTIONS. **NEIL TYLER REPORTS** 

Qualcomm Technologies has launched a family of 60GHz Wi-Fi chipsets, the QCA64x8 and QCA64x1, that are able to deliver 10+ gigabit-per-second (Gbps) network speeds and wire equivalent latency, while setting an industry low-power benchmark for extended device battery life.

With the reliance on high-bandwidth mmWave spectrum set to increase, this 60GHz Wi-Fi portfolio has been designed to provide greater flexibility while harnessing a range of capabilities that will support new 60GHz Wi-Fi sensing applications like proximity and presence detection, gesture recognition, room mapping with precise location and improved facial feature detection.

Qualcomm is the first-to market with a 60GHz Wi-Fi solution with optimisations based on the 802.11ay specification, enabling best-in-class 60GHz Wi-Fi speeds and much improved coverage performance.

"mmWave holds enormous potential to support a new class of user experiences," said Rahul Patel, senior vice president and general manager, connectivity and networking, Qualcomm Technologies. "Our 11ay solutions were developed to support a broad ecosystem of smartphone, router or fixed wireless access platforms and provides the industry with the building blocks needed to take connectivity performance to the next level."

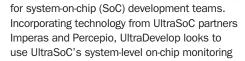
The 11ay 60GHz Wi-Fi chipsets includes QCA6438 and QCA6428 for infrastructure and fixed wireless access, and the QCA6421 and QCA6431 for mobile applications.

mmWave-based 60GHz Wi-Fi is a low interference, bandwidth rich spectrum that delivers increased wireless capacity, multi-gigabit speeds, and ultra-low latency and so is suited to a wide range of wireless ecosystems spanning mobile, enterprise, outdoor backhaul, and the smart home.

The performance of 60GHz Wi-Fi goes far beyond high performance throughput, as the new chipsets will also enable always-on ambient Wi-Fi sensing capabilities, enabling devices to identify people, objects, movements and precise location without being affected by light conditions.

#### UltraSoC extends tools suite

UltraSoC has launched a new tool suite. The UltraDevelop 2 is a complete integrated development environment (IDE) that combines debug, run control, and performance tuning with advanced visualisation and data science capabilities





and analytics infrastructure, to cut development costs, shorten time-to-revenue and improve product quality.

The tools suite delivers a holistic, system-level approach to SoC development and debug, allowing engineers to view and analyse the interlinked behaviour

of hardware, firmware and software at any level of abstraction - and to interactively switch between views and tools depending on the task

#### Arm's DesignStart now includes Cortex-A5

Arm is expanding the DesignStart programme to include the Cortex-A5. DesignStart is intended to make prototyping easier for design engineers.

The Cortex-A5 is a high-performance, feature-rich processor intended for cost-sensitive applications with advanced requirements across a range of diverse markets such as medical, smart home and industrial.

DesignStart looks to provide fast, easy access to the Cortex-A5 processor through a web portal and a simplified contract, speeding up time to market. Its small footprint (<0.3mm when implemented on a 40nm process) and ultra-high efficiency (~100uW/MHz active power when implemented on a 40nm process) allows for reduced fabrication costs and the lowest idle power among Cortex-A CPUs.

### Simplifying IoT

myDevices and Arm have joined forces to accelerate the creation of finished IoT solutions by simplifying device onboarding and increasing the number of sensors, gateways, and solutions integrated with the Arm Pelion IoT Platform

myDevices has partnered with gateway and sensor manufacturers to create an extensive ecosystem of LoRa devices that can be easily mixed and matched to create specific vertical applications.

myDevices provides IoT enablement such as QR code onboarding, permission-based user management, escalations, threshold alerts, time-based rules, reporting, corrective action logs, device history visualisation, and 3rd party integrations, which are all accessible from native mobile apps, an online dashboard, or an API.

"In addition, Arm's device management provides secure FOTA updates to these solutions, while its data management provides enterprise level insights," said Kevin Bromber, Founder and CEO of myDevices.

#### **Apple hires Dialog** engineers

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# Recycling expensive wafers now possible

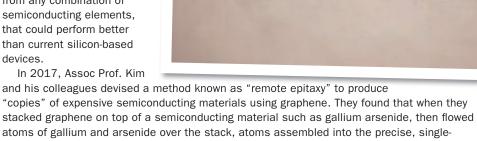
SEMICONDUCTING FILMS FROM EXOTIC MATERIALS OUTPERFORM SILICON.

**BETHAN GRYLLS REPORTS** 

A technique to fabricate ultrathin semiconducting films made from gallium arsenide, gallium nitride, and lithium fluoride has been developed by MIT engineers.

The new technique, according to the researchers, provides a cost-effective method to fabricate flexible electronics made from any combination of semiconducting elements, that could perform better than current silicon-based devices.

In 2017, Assoc Prof. Kim



"copies" of expensive semiconducting materials using graphene. They found that when they stacked graphene on top of a semiconducting material such as gallium arsenide, then flowed atoms of gallium and arsenide over the stack, atoms assembled into the precise, singlecrystalline pattern of the underlying semiconducting wafer, forming a copy that could be peeled away.

The team then tried applying remote epitaxy to silicon and also germanium, but found that when they flowed these atoms over graphene they failed to interact with their respective underlying layers. Perhaps, the team reasoned, atoms can only interact with each other through graphene if they have some ionic charge.

The researchers tested their hypothesis by using remote epitaxy to copy semiconducting materials with various degrees of polarity, from neutral silicon and germanium, to slightly polarised gallium arsenide, and finally, highly polarised lithium fluoride.

They found that the greater the degree of polarity, the stronger the atomic interaction, even, in some cases, through multiple sheets of graphene. Each film they were able to produce was flexible and merely tens to hundreds of nanometers thick.

The team also experimented with an intermediate layer of hexagonal boron nitride (hBN) which is made of oppositely charged boron and nitrogen atoms that generate a polarity within the material itself. In their experiments, they found that any atoms flowing over hBN. even if they were highly polarised themselves, were unable to interact with their underlying wafers completely. This suggested that the polarity of both the atoms of interest and the intermediate material determines whether the atoms will interact and form a copy of the original semiconducting wafer.

With this new understanding, the researchers can now look at the periodic table and pick two elements of opposite charge. Once they acquire or fabricate a main wafer made from the same elements, they can then apply the team's remote epitaxy techniques to fabricate multiple, exact copies of the original wafer.

"People have mostly used silicon wafers because they're cheap," says Associate Professor Jeehwan Kim of MIT. "Our method opens up a way to use higher-performing, nonsilicon materials. You can just purchase one expensive wafer and copy it over and over again, and keep reusing the wafer."

**5G problems** 

# SECURITY GAPS IN THE 5G MOBILE COMMUNICATION STANDARD UNCOVERED. BETHAN GRYLLS REPORTS

5G is looking to offer users more security than before, but in order to assure it, the device and network must be able to authenticate each other, and the confidentiality of the data exchange and the privacy of the

user concerning identity and location must be guaranteed.

This has been implemented through a protocol known as Authentication and Key Agreement (AKA) since the introduction of the 3G standard.

With the aid of the security protocol verification tool Tamarin, an ETH research team systematically examined the 5G AKA protocol, taking the specified security aims into account.

According to ETH, Tamarin was developed and improved during the last eight years in this research group and is one of the most effective tools for analysing cryptographic protocols. The tool automatically identifies the minimum-security assumptions required in order to achieve the security objectives set by 3GPP.

"It showed that the standard is insufficient to achieve all the critical security aims of the 5G AKA protocol," says senior scientist and co-author Ralf Sasse. "It is therefore possible for a poor implementation of the current standard to result in users being charged for the mobile phone usage of a third party."

As the team determined, data protection will be improved significantly with the new protocol in comparison with 3G and 4G technologies. In addition, 3GPP succeeded in closing a gap with the new standard that had previously been exploited by IMSI catchers. With these devices, the International Mobile Subscriber Identity (IMSI) of a mobile phone card can be read to determine the location of a mobile device.

To achieve this, the device masquerades as a radio station in order not to be caught by the mobile phone. "This gap is closed with the 5G AKA. However, we have determined that the protocol permits other types of traceability attacks," explains senior scientist and co-author Lucca Hirschi

## A smart collaboration

The Centre for Process Innovation (CPI), a UK-based technology innovation centre, is working with Pireta to scale-up wearable technology in textiles.

CPI is coating individual fibres with metal on fabrics in selective patterns without changing its physical and mechanical properties. This enables wearable electronics to be more discreet as the electrodes are integrated into the fabric.

With its expertise in hybrid and stretchable electronics, CPI is supporting Pireta's work on developing a process that will make it possible to make durable, flexible, interconnecting electrodes that avoid changing fabric feel and performance.

Employing proven aqueous processes and commercially available chemistries, Pireta has a track record of producing highly conductive, robust and complex circuit demonstrators on a variety of textiles. This gives the textiles a low sheet resistance, a conductor that does not crack, and flexibility, breathability and performance that is maintained when washed or stretched.

The project, known as TexAnn, aims to significantly reduce existing manufacturing timescales while optimising electrode pattern resolution.



The Department for Digital, Culture, Media and Sport (DCMS) and the National Cyber Security Centre (NCSC) have set out plans in a Secure by Design' review to embed security in the design process of new technology rather than bolt it on as an afterthought.

As a result, a new Code of Practice has been developed with industry to improve the cyber security of devices, encourage innovation in new technologies, and keep consumers safe.

The new Code of Practice outlines 13 guidelines that manufacturers of consumer devices should implement into their product's design to keep consumers safe. This includes secure storage of personal data, regular software updates to make sure devices are protected against emerging security threats, no default passwords and making it easier for users to delete their personal data off the product.

Implementing the Code of Practice can help organisations make sure that smart devices that process personal data are compliant with the stronger data protection laws which came into force in May. Failure to comply with the General Data Protection Regulations means firms could risk fines of up to £17m or 4 percent of global turnover, for the most serious data breaches.



### Brighton testbed looks to showcase 5G technology

LAST MONTH A UK 5G TESTBED WAS LAUNCHED TO SHOWCASE SOME OF THE LATEST INNOVATION AND IMMERSIVE TECHNOLOGIES. **NEIL TYLER** REPORTS

ast month the UK's Digital Catapult, Coast to Capital LEP, Wired Sussex, and the University of Brighton came together to launch FuseBox in Brighton.

The new 5G testbed is intended to allow small businesses, based in and around Brighton on the UK's south coast, to benefit from 5G mobile wireless communications, and provide a space to test and explore potential applications associated with 5G.

The facility looks to provide an environment where start-ups and scaleups can access "the most advanced digital technology solutions", including an Immersive Lab, designed to help these businesses grow faster.

Digital Catapult and its partners are encouraging local companies to register to take part in using the testbed to develop their ideas and it's intended to help meet the commitment, made in the Government's Industrial Strategy, calling for the UK to become a world-leader in 5G technology.

Commenting Dr Jeremy Silver, CEO, Digital Catapult, said: "The 5G Brighton testbed will let companies experiment with new applications and services which take advantage of the unique nature of 5G. This is a major step forward in the wider roll out of this advanced technology, helping take the technology out of university labs and into the market."

Speaking about the testbed to New Electronics Dritan Kaleshi, Lead Technologist (Future Networks, 5G Fellow), Digital

Catapult, said, "This is a significant development. It's the first time that a testbed has been developed to specifically see how we can bring innovation programmes and SMEs together, to not only better understand the technology, but see how companies engage with 5G and how they can use it to better align their technology roadmaps."

The UK government's ambition to make the UK a world leader in 5G saw the

"This is a significant development.
To see how companies engage with, and use, 5G."

publication, earlier this year, of the UK 5G Strategy report. Produced by the Digital Catapult it said that there was a clear recognition that a world-class digital infrastructure was a critical building block when it came to creating new opportunities for growth by 'enabling new business models, opening up

new opportunities for innovation and driving productivity across the economy.'

"5G offers significant opportunities for the UK, leading to new and imaginative deployment models across the spectrum," said Kaleshi. "While we don't have the manufacturing interests in 5G that economies like China and South Korea have, the UK is a world leader in terms of system architectures, systems integration, application development, cyber security and academic research into communications."

According to Kaleshi, the UK's 5G ecosystem, "Has real momentum going forward and is highly interconnected. It is composed of a wide and diverse range of players, from private sector companies, academic and research organisations, through to public-sector bodies."

This ecosystem is growing around core stakeholders, with testbeds and trials already taking place and the UK is, according to Kaleshi, "largely in line with other leading countries efforts in 5G." In fact, it is ranked alongside Germany as being among the top 5 economies engaging with 5G.

"Activities in the UK span the entire mobile and wireless infrastructure and involve individual mobile technology blocks and software as well as end-to-end network system integration and testbeds," said Kaleshi. "We believe that the testbeds that are appearing in the UK will ultimately scale-up to become fully deployed solutions."

Further success will be reliant, however, on the ability to cross-innovate between academia, innovators and industry, where UK-bred R&D in 5G can be developed into real world deployable applications.

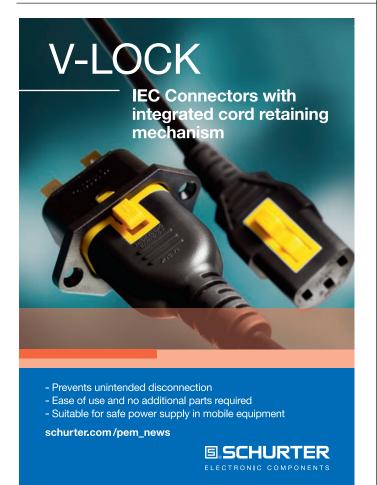
There are a number of key areas that have been identified as benefitting from the advent of 5G including manufacturing, healthcare and transport.













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otography Karla Gowlett

hen it came to this year's British Engineering Awards, held in London earlier this month, the question when judging entries was "What have they given back?"

The winner of this year's Grand Prix, AESSEAL, has – for nearly twenty years – worked tirelessly to help young people see engineering as a possible future career path.

As Winner of the Engineering Ambassador of the Year, AESSEAL duly went on to win the Grand Prix, Best of the Best award, for encouraging increased interest in engineering and promoting the uptake of STEM subjects.



# Bridging the gap to the future

Engineering outreach and engagement is in the company's DNA and is embedded in its working life at every level.

The first known record of AESSEAL working with students to promote engineering came in 2002, when it sponsored 4,000 sets of 3D CAD software that were made available to local schools, colleges and Sheffield Hallam University as part of the Back to Grass Roots campaign.

Last year the company engaged with 2,250 students, including 190 directly involved in its in-house outreach work with visits to schools and student visits to AESSEAL. This year it has had contact with 2,840 students to date, of which 640 were directly involved in its in-house outreach work.

Its apprentices visit schools to

give 'A day in the life'- type talks to students preparing to make choices about their careers - bringing a career in engineering to life and making it a far more attractive prospect to young people yet to experience the world of

AESSEAL also funds four engineering bursaries at Sheffield University, donating £50,000 to the university to support its 'Engineering Is' campaign. This looks to create a step change in attracting women into engineering through work with primary schools, funding a physics bridging course for female A-Level students, and supporting female engineering academics to progress into professorial roles.

The AESSEAL Manufacturing
Apprenticeship programme in
Rotherham was developed in specific

When it comes to engineering outreach, AESSEAL puts its money where its mouth is and proved a worthy Grand Prix Winner. By **Neil Tyler** 

response to the engineering skills shortage. It was launched in 2012 in partnership with the University of Sheffield's Advanced Manufacturing Resource Centre (AMRC) and is run in collaboration with the AMRC and Rotherham College.

#### The judges said:

"It's time to recognise the work of a company that, since 2002, has worked with the wider community to promote engineering, reaching out to thousands of potential young engineers."

Engineering Ambassador of the Year Highly Commended:

TDK-Lambda UK

#### **Consultancy of the Year**

Sponsored by: Rutland Plastics

#### **Stirling Dynamics**

Taking a highly-collaborative approach

## COVER STORY O BRITISH ENGINEERING EXCELLENCE AWARDS

to its clients and designs Stirling
Dynamics works in the aerospace
sector, designing and modifying
aircraft and components. Stirling has
evolved from being very UK-centric
and reliant on one key customer to
become an international consultancy
servicing multiple customers.

The company follows a "Customer Friendly" business model which is one of its strongest USPs. Stirling is unafraid of sharing IP and knowledge transfer with its customer base. The trusted relationships that it's built have resulted in repeat business.

The company's recent success brought it to the attention of Assystem Technologies UK, who acquired Stirling Dynamics in April 2018.

#### The judges said:

"Delivering a range of complex systems and technical services, the company's track record of expanding into overseas markets is truly impressive."

#### **Small Company of the Year**

Sponsored by MA Business

#### **Transmission Dynamics**

A change of strategy from mechanical to IoT solutions has reaped dividends for Transmission Dynamics.

Established in 1996 as JR
Dynamics, since 2006 it has traded as Transmission Dynamics and established itself as a condition monitoring specialist that uses IoT to deliver critical data and reports related to client assets in real time.

By persevering with innovation and creativity, combined with the unique talent, enthusiasm and hardworking of its key staff, TD is now an innovative and fast-growing SMEs in a global market.

This ability to design products from concept to fruition has allowed TD to maintain control over product development right through the product life cycle.

#### The judges said:

"This was a terrific example of how

to take a technology developed in academia, and use it as the basis of a highly successful and flourishing business."

### Highly Commended: Synergie Environ

#### Start-Up of the Year

Sponsored by Cambridge Consultants

#### Circuitworx

Specialising in helping its fellow start-ups bring products to market, Cicuitworx has enjoyed exceptional growth.

Many start-up companies lack the wider technical expertise, systems engineering knowledge or commercial experience to develop their ideas further and this is where CircuitWorx comes in, designing bespoke electronics and software, managing subcontractors and working with the client through the whole product development lifecycle.

This integrated whole-lifecycle engineering design service allows the client to focus on its strengths and wider business objectives being confident in the quality of the technology designed/manufactured by CircuitWorx, resulting in the client's product being successfully brought to market.

#### The judges said:

"The company has demonstrated a strong track record, delivering exceptional growth and

profitability, based on its ability to provide innovative solutions."

#### **Design Team of the Year**

Sponsored by LG Motion

#### Imagination

#### **Technologies**

A team consisting of 90 engineers spread across four countries were able to deliver, in just 14 short months, the PowerVR Series2NX neural networked accelerator (NNA). Delivering Below: Grand Prix Winners, ASSEAL. Collecting the award, David Amory, Global Marketing Director and Rebecca Clubbe, Marketing Communications Manager high-performance computation of neural networks at very low power consumption in a minimal silicon area, the 2NX was designed from the ground-up to provide hardware acceleration for efficient neural network inference in mobile/ embedded platforms.

With flexible bit-depth support on a per-layer basis for weights and data, it can maintain high inference accuracy while drastically reducing bandwidth/power requirements.

It is the only solution supporting bit-depths from 16-bit (required for automotive), to 4-bit, resulting in higher performance at lower bandwidth and power. A single core of 2NX, running at 800MHz, offers up to 2048 MACs/cycle.

#### The judges said:

"A hard-working team that, despite being geographically dispersed, came together effectively to deliver a complex product in a short amount of time."

#### **Electronic Product of the Year**

Sponsored by TÜV Sud

#### Xilinx

The data and power demands of 5G networks require a special product to satisfy them.

In response, Xilinx conceived the RF System on Chip (RFSoC) to deliver previously unachieved levels of

integration, leveraging its advanced 16nm FinFET process to let analogue functions benefit from the pace of CMOS technology advancement, and so overcome the power and size challenges presented by Massive MIMO.

The key innovation, enabling RF and analogue circuitry to be brought on-chip, is direct RF sampling. This was achieved by Xilinx leveraging its Zynq UltraScale+ MPSoC to provide a proven launchpad. As a result, the RFSoCs



## COVER STORY BRITISH ENGINEERING EXCELLENCE AWARDS

monolithically integrate RF data converters and soft-decision Forward Error Correction (SD-FEC) cores are able to meet 5G and DOCSIS 3.1 standards using the 16nm Zynq UltraScale+ MPSoC architecture.

As a market-ready product, RFSoC brings together several technical threads, encompassing digital, analogue and RF chip design, as well as soft IP blocks, and device drivers, and customer development tools.

Working with leading infrastructure makers and network operators to ensure RFSoC meets all the needs of 5G stakeholders, Xilinx produced test chips for evaluation in customers' programmes.

Roll-out was then expanded to 20 customers, in preparation for general availability on the market in 2018. **The judges said:** 

"This provides a key enabling technology for the future roll-out of 5G. Xilinx has deployed a variety of innovative techniques to overcome a range of technical challenges."

#### **Young Design Engineer of the Year**

Sponsored by RS Components

#### Brent Brakeboer, Surrey Satellite Technology

The UK satellite industry is no easy place to make your mark, but this year's winner has done that and more.

In two years Brent Brakeboer had a huge impact on Surrey Satellite Technology having driven the internal development of the next generation of Earth Observation medium resolution wide swath multi band camera systems to replace and upgrade the ageing Rapideye spacecraft system.

Leading the whole design from scratch through to delivery, Brent engaged with subcontractors and suppliers, brought new suppliers into space activities and passed on knowledge of SSTL's requirements to allow them to improve their designs and expand their businesses into new engineering fields.

Brent's has de-risked a significant programme for SSTL in advance of the

main project and has strengthened the position of the company to provide another world class mission to the market place, bringing tens of millions of pounds of work to the UK space sector.

#### The judges said of Brent:

"Showing exceptional skills as well as initiative in solving problems, Brent came up with a truly exceptional and differentiated product."

#### **Highly Commended:**

Callum Bramley, Respond

#### **Design Engineer of the Year**

Sponsored by Maxon Motor

#### Orlas Murphy, Jaguar Land Rover

A multi-talented, multi-disciplinary engineer since joining Jaguar Land Rover in 2012, Orla has progressed through different roles in both the Electrical Engineering and Vehicle Engineering departments.

She has worked in the audio team, calibrating the sound systems within the vehicles, using analytical, acoustic and both objective and subjective testing skills.

In the Quality team, she works on complex problem solving for warranty issues. However, over the last year her work in a design role has focussed on a study into Automotive Software Overthe-Air (SOTA), which she led as a joint research project between Jaguar Land Rover and the University of Bradford.

Orla has won numerous awards

Below: Orla Murphy (centre), Design Engineer of the Year



and, as a STEM ambassador, gives technical lectures on her work for all ages, from school children up to retired engineers.

#### The judges said:

"Orla has come a long way in a relatively short space of time, having progressed through the company in a variety of roles."

#### **Materials Application**

Sponsored by Goodfellow

#### **Nylacast Chock Liner**

The Chock Liner by Nylacast is an evolution in mooring technology.
Custom manufactured from initial chemistry to end product, the patented Chock Liner delivers safe and reliable moorings by using the advantages of its custom formulated Polyamide 6 material with very low friction properties in order to line the often rough, worn and rusted chocks (or panama fairleads) on vessels.

#### The judges said:

"A classic example of the right material finding the perfect application to create a successful product."

#### **Mechanical Product of the Year**

Sponsored by Minitec

#### Aeristech

Aeristech has invented a new motor control technology, Aeristech Control Technology, ACT making possible a variable speed electric motor more power dense than any other in the world.

To suit the needs of fuel cells it developed an air compressor, FCC, superior in every respect to any other in the market.

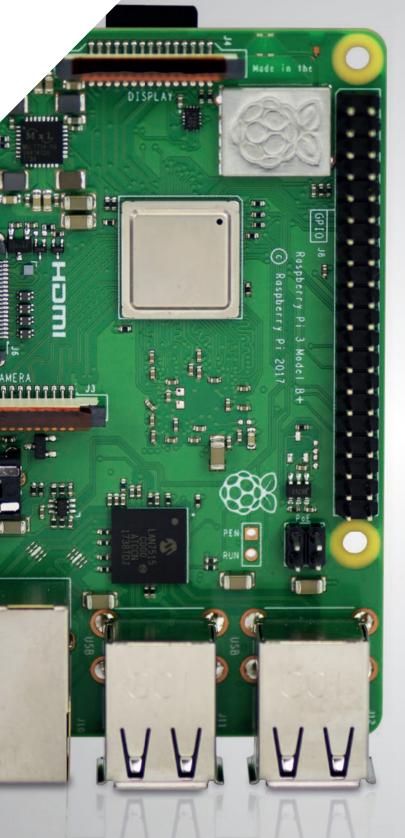
Supported by an "Advanced Propulsion Centre" and an "EU Horizon 20/20 grant" for re-engineering the device for mass production and developing a bill of quantities, the launch of the Aeristech FCC supplying a 120kW+ fuel Cell powering a vehicle demonstrator is scheduled for summer 2019.

#### The judges said:

"Aeristech impressed with its response to a real market need and is set for real commercial success."







## WHERE INNOVATION HAS NO LIMITS

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q electronica 2018

e live in a spatial world, but so far, education appears to be constrained to 'flat', 2D experiences, such as books and screens. According to educationalist, Edgar Dale, we retain around 10% of what we read, compared with 90% of what we experience ourselves.

The promise of virtual (VR) and augmented reality (AR) has yet to break the conformity of 'flat learning', but according to Dave Chavez, CTO of ZSpace, that's all set to change with the development of what the company says is the world's first AR/VR laptop.

"Our technology takes advantage of the spatial world, and our senses, and enables a means to interact in a much more natural way," Chavez says.

According to Chavez, it's a more engaging learning practise because it's immersive, and allows the user to study in a way that engages all of their senses.



# Reinventing flat education

So far traditional schooling has been restricted to the 2D screen or textbook. Now, ZSpace looks to give it a push into the 21st century. By **Bethan Grylls** 

"We placed audio into the laptop and a haptic transducer into a stylus. So, for example, students can not only view and study a human heart in 3D, but also hear and feel it beating."

According to a report from the American Optometric Association, "The educational benefits of presenting teaching materials in 3D are promising, generating a significant improvement in comprehension and retention over the more traditional non-3D style of presentation."

The ZSpace system opens up possibilities that weren't achievable before, says Chavez. "You can do things that aren't so easy to do or not possible in real life. For example,

zooming in and studying a 3D structure of DNA."

The idea to place the ZSpace system in the classroom, however, was not the original drive for the company. Instead, the initial goal was to create a "comfortable" 3D display.

Previously, 3D systems used Cathode Raid Tubes (CRTs) and shutter glasses comprising active electronics. The CRT contained an electron 'gun' which modulated, accelerated and deflected the electron beam that emanated from it onto a phosphorescent screen. The electronics in the glasses had polarisers that opened and closed, cutting the light off completely in one

Above: ZSpace has created what it says is the first AR/ VR laptop eye and then the other. This allowed for different images to be delivered to each eye, creating a sense of 3D depth. LCDs later replaced CRTs, but it wasn't generally accepted as a "comfortable" solution due to the flickering visuals, suggests Chavez.

"We asked ourselves, how could we create a really comfortable 3D display system using LCD? And one of the questions that sprung from that was 'how will people use it?' It seemed that other work was mostly aimed at high-end applications and focused in the scientific and medical industries. As we created ZSpace, we saw there was a much broader application – schools," he says.

#### DESIGN PLUS VIRTUAL EDUCATION

Chavez believes that the traditional flat way of learning is only accepted because there's no other option and the options that do exist are either uncomfortable, ask too much of the user, or are expensive.

"If, in the future, you didn't have to wear glasses and screens were volumetric like the rest of the world, people would readily accept this as the norm."

To create its 'comfortable' solution, Chavez says ZSpace "took a risk", steering away from traditional 'active' – that is electronics within – glasses, and instead created a passive pair.

ZSpace then integrated all of the necessary components into a bespoke laptop for a lighter, more comfortable wearable experience, says Chavez.

"We didn't want to build a super custom laptop that was going to cost a fortune," continues Chavez. "We started with a basic laptop design and worked with AMD to pick a processor and GPU that was going to able to deliver this experience. Essentially, it's a Windows 10, but just a little heavier."

#### **Polarisation**

To create the perception of 3D, ZSpace used polarisation.

"Natural light is comprised mostly of randomly polarised light; a mixture of degrees of vertically and horizontally polarised light of varying magnitudes and angles. Vertically and horizontally polarised light are special cases, where the electromagnetic lines have been aligned," explains Chavez. To visual it, imagine a ribbon (representing light) being waved up and down and then side to side.

"Circularly polarised light is another special case," he adds, "where the phase relationship of the electromagnetic waves results in the direction of the electric field to vary in time."

The ZSpace glasses are

oppositely polarised – one left-circularly-polarised, the other right-circularly-polarised. To track the user's eye position and orientation, IR cameras are built into the laptop. Using polarisation, the glasses transmit the correct display image and block the image intended for the opposite eye.

The tracking system allows the graphics engine to render correct projections in real time, based on the user's viewing position.

On the laptop, there is an active layer of electronics in the display, explains Chavez. As the images 'shoot' from the GPU at 120fps, the display system alternates between left circular polarisation and right circular polarisation, with the intention to deliver them to the left eye, then the right, then the left etc. Thus, with binocular vision, simulating the way in which we view real life objects.

The cameras in the laptop track the markers on the glasses and stylus provided with the ZSpace system. The markers reflect IR from emitters which are placed close to the cameras. This allows the camera system to determine the position of the glasses and stylus.

"We're heading into a world where screens won't be flat, where the web won't be flat - and we're going to be a big part of that, if not the leaders."

for the system needed to be low, so the tracking system had to be able to detect position within milliseconds. The IR helped the team to accomplish this as it filters out visible light, allowing the camera to focus on what it needs to. "The imagery was reduced to dots and then further reduced to a list of x and y coordinates. That's not very much information at all, so it allowed for a very fast system," says Chavez.

Chavez explains that latency

#### **Future**

With AR/VR dipping in and out of the limelight, Chavez did admit that initially, it concerned him it was "just a fad". However, after developing ZSpace he says his worries have disappeared. "We have created something really special," he says.

"Part of that," he adds, "is because we have developed a hasslefree and less expensive solution with lots of benefit to the user. That's why it's not caught on before, we have been asking too much with little to give in return."

As for the future, Chavez believes ZSpace has plenty of industry opportunity.

"I can see people shopping and communicating this way. We're working with Google and the Chrome browser at the moment."

Despite not being able to reveal specifics of this joint project, Chavez did hint at the notion of a 3D web browser. "We're heading into a world where screens won't be flat, where the web won't be flat and we are going to be a big part of that."

Although we are yet to see definitive studies detailing the benefits and results of long term use of VR/AR in education, most research concludes that engagement and user reactions has been positive.

So, we'll just have to wait and see whether schools take note, or if like other virtual technology, it's just a matter of time before it peters out and it's time to hit the books again.

Below: All the
ZSpace components
are built into a
custom laptop,
with the glasses
remaining
passive for a
more comfortable
experience











November 13-16, 2018

# Connecting everything – smart, safe & secure

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- electronica Careers





# **Just Connect**

As exhibitors and visitors prepare for electronica, **Bethan Grylls** looks at how the event has grown and what we can expect to see in Munich

he already impressively sized electronica returns this November 13-16, with 8,000m<sup>2</sup> more space than 2016's exhibition.

With the addition of two newly constructed halls (C5 and 6), electronica has sought to expand further and will now occupy 17 of the 18 halls at the Messe in Germany, Munich.

This year's event will also see an increased number of forums, and a new medical conference – eMEC – that looks to bring together practitioners from everyday medical treatment with specialists from the electronics industry.

While popular conference topics such as IoT and cybersecurity will be returning they will be joined by newly added ones, covering smart grid and smart energy, as well as artificial intelligence (AI).

The reasoning behind the expansion is not only as a result of last year's demand for more space, according to Angela Marten, Messe Muchen, Exhibition Director, but comes in response to this year's theme of 'Connecting everything – safe, smart and secure'.

"We want to connect the industry and provide an opportunity for visitors to really 'experience' the electronics sector," said Marten. She explained that the extension has made room for new additions which she hopes will help deliver this intended experience, including the premiere of the 'electronica experience' in Hall C6.

"We've discovered that our exhibitors tend to showcase their products by means of their application," she explained. "So, we wanted to offer exhibitors a



central space to do this, as well as an opportunity to increase brand visibility."

Marten explained that the idea evolved with the electronica experience becoming a career space for companies to target young talent. There is a significant skills gap, Marten contended, and through this careers section she hoped electronica would not only encourage students into the sector, but introduce them to a thriving industry.

"The electronica Experience is a particularly exciting addition," said Kurt Colehower, President Global Sourcing at RS Components. "It's critical that we all do whatever we can to engage and inspire the next generation towards considering engineering as a career. We face an engineering skills deficit across Europe and a continued decline could have serious implications for the European economy.

"RS will be bringing along Titan II, our 35-tonne technology-filled truck, which tours schools and events giving children and young people the chance Above: Analog
Devices will be
among the many
exhibitors at
electronica 2018,
using the show as
an opportunity to
demonstrate a range
of application demos
in the industrial
space

"We want to connect the industry and provide an opportunity for vistors to really 'experience' the electronics sector Angela Marten to get hands-on with the technology."

RS has also teamed with electronica on the Big Step Challenge, focusing on the event's theme of connecting. The aim is to walk the distance from each exhibiting country's capital to the exhibition in Munich. "The challenge has been devised to harness the power of the show's international audience," said Colehower. As each 100,000,000 step milestone is achieved, the organisers will donate FIRST LEGO League kits to community groups across Germany.

At the heart of the electronica experience is the Discovery Stage, explained Marten, which will feature talks, presentations and panel discussions on trending and future topics, including blockchain, smart factories and Al.

"electronica always follows industry trends, looking at what is the 'talk' of the industry – and that is reflected in our conference topics," said Marten. "E-health is predicted to grow at impressive rates," she said, pointing to the new eMEC conference as an

#### ELECTRONICA ( ) SHOW PREVIEW

example of electronica's ability to mirror key industry movements.

electronica fast forward (ee-ffwd) will return with a new sponsors challenge. This gives start-ups the possibility to develop their product with designated hardware provided by the sponsor. For example, developers were asked to create innovative designs using Arrow development boards. The winner and best three designs will be on view at Arrow's booth.

According to Marten, the expansion of electronica has also seen a shift in layout, with semiconductors in halls A4, B4, C4 and the adjacent halls B5, C5 and C3. A co-located event, SEMICON Europa, will take up part of hall A4. The automotive and embedded systems segments and, directly adjacent to them, displays and sensors are also moving.

"Electromechanics/system periphery, relays and casing technology are another segment that take up more than two halls, which is why we have chosen a north to south arrangement on the grounds for this as well," Marten added. "From 2018, exhibitors from these areas will be in halls A2, B2 and C2. Circuit carriers and EMS will move to halls A1 and B1, and passive components to A6 and B6. As a result, the remaining areas will move too."

Despite the layout changes, Marten believes electronica will be easy to navigate, with colour coded segments acting as a guide for visitors. The show has been organised in a more logical way, so that, where possible, neighbouring topics have been positioned next to one another.

"The sheer scale of electronica gives us a chance to meet the majority of our suppliers in one place, as well as our existing and potential new customers," added Martin Keenan, Technical Director at Avnet Abacus, expressing the general consensus among exhibitors of the idea of a bigger electronica. "The exhibition is a real barometer for the industry. The fact that it is growing is a testament to the proliferation of electronics."

Following the theme of 'experiencing electronics' that Marten described, Avnet Abacus will be using electronica to showcase six live examples of finished products at its booth. These will all be projects it helped to develop and bring to market. "We will be telling the stories behind each product, explaining how we overcame specific challenges," explained Keenan. "We believe this will bring to life what we do every day and demonstrate what we do beyond being a distributor and the value we bring to the end-customers."

"electronica is an important fixture



Above: One of the key product demos for Avnet Abacus will be Hanhaa's live parcel tracking service, which allows users to determine the exact location and condition of their parcel in real time anywhere in the world

in the calendar," Colehower added, "It is a great opportunity for us to meet with our most important customers and suppliers over the course of four days, and to build on those relationships.

"It's great to see the event continuing to expand. I think this sends a positive message for our industry."

"Exhibitors are growing constantly," Marten said. "This year we have 10,000sq metres net more than we had in 2016. We have an increase in terms of net space by almost 20 per cent between 2014-2018.

"As for the future, electronica will continue what it's doing – it's not all about space," she admitted. "What's more important is what the show is about and what the benefits are for those attending." She explains that the intention this year is to offer more benefits than previous shows, with this theme of 'connecting and experiencing' as its main focus.



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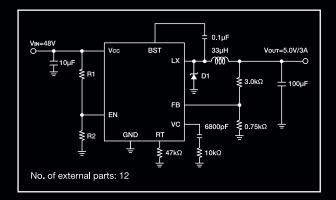


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#### **FEATURES**

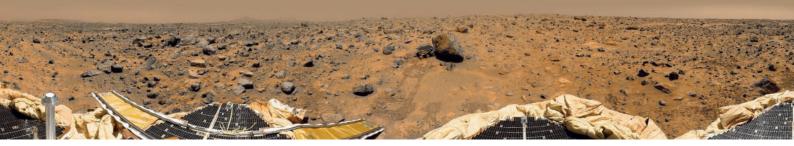
- Input voltage range: 12V to 76V (80V max.)
- Output voltage range: 1.0V to VCC V
- Reference voltage: 1.0V±1.5% (25°C) ±2.0% (-40°C to 85°C)
- Operating frequency: 50 to 750kHz (typ.)
- Maximum output current: 3.0A
- EN pin threshold: ±3%
- Soft start function
- Protection Circuit: OCP, UVLO, TSD, OVP
- HTSOP-J8 package (4.9×6.0×1.0mm)



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# Loose threads

As IoT and distributed cyber-physical systems become more sophisticated, timing is proving increasingly difficult to manage. By **Chris Edwards** 



iming can be tricky in embedded systems. Shortly after it touched down on the surface of Mars in 1997, NASA's Pathfinder lander started to malfunction, triggering a watchdog timer that engineers tried to fix with system resets. There was no actual bug in the lines of code that controlled the robot. Instead the bug was lurking in the way the different tasks interacted with each other.

To complete its work each cycle, a management task needed access to the system bus. But it was being locked out by a weather-monitoring thread that needed access to the same bus. Because it would often get pre-empted by a long-running communications task, the weather thread failed to finish and release the mutual-exclusion semaphores that gave it access to the bus. Without access to the semaphore and the bus, the management task missed its deadlines repeatedly: an example of priority inversion. A change to the way locks are managed in the kernel fixed the problem in perhaps the prime example of long-distance bug-fixing.

Now, two decades on, cloudcomputer operators are struggling with odd holdups in their systems – a phenomenon known as tail latency. Most tasks complete without a hitch in a matter of seconds. But a few get held up for much longer with no readily apparent cause. The software was the same; the requests being made to the servers were not unusual. They just had to wait a very long time to be serviced.

#### **Growing sophistication**

As IoT and distributed cyber-physical systems become more sophisticated, embedded systems designers are increasingly likely to be faced with the problems caused by scheduling issues from very different systems. At one end are the interactions between tasks caused by threads holding on too long to exclusive resources in a single device. At the other is the unpredictable tail latency that afflicts applications that do not exist in a single node but which are spread across many nodes, both local and in the cloud. In the middle are the performance issues caused by interactions between threads, the operating system, hypervisors and the processors and memory on which they

A big difference between the kind of processor used in Pathfinder and those now employed in robotic controllers and cloud computers is the use of multiprocessing and caching. Both can affect the performance of the synchronisation techniques needed in multitasking systems. Such synchronisation is vital because different task loads can let one thread easily race ahead of another if not

Above: A 360° Gallery Pan, the first contiguous, uniform panorama taken by the Imager for Mars checked. Resource locking and thread synchronisation prevent memory and I/O ports from handling corrupt data.

If a lot of threads need to read data from the same location, a mutex of the kind used in the Mars Pathfinder tends to hurt performance. So, a broad range of techniques have emerged that fall under the banner of lock-free synchronisation. In these the application is structured so that a lock is only needed to complete a write operation or takes advantage of atomic operations where the memory is not released until the write is completed.

However, interactions between applications and more advanced locking strategies can still lead to unexpected sudden delays for unlucky threads – showing up in logs as excessive tail latency. For example, to obtain a lock, a thread has to "spin" on it – testing its status until it is free. These memory accesses can slow down other threads that have no logical connection because of interactions between the memory and the various caches inside the system.

Very often in high-performance multicore SoCs, the locks will be cached and the cache-coherency mechanisms used to ensure processors that cannot see inside the cache are updated properly. If locks and regular data lie on the same cache line, the threads accessing

#### EMBEDDED DESIGN () EMBEDDED TEST

that data can have their performance degraded through continual cache-coherency updates. Simply reorganising memory can cause this problem to disappear. That is one reason why tail latency and similar problems can be hard to track down.

Since the Pathfinder missions, a number of tools have appeared that are designed to help embedded-systems designers sift through the mountains of data needed to get a picture of what is happening inside a single system. As IoT and distributed cyber-physical systems take hold, similar but larger-scale tools are beginning to appear.

Green Hill Systems was one of the early converts to the idea of making it easier to analyse embedded-systems performance using different perspectives. Fifteen years, alongside a debugger that could work backwards along a timeline from a fault, the company introduced the PathAnalyzer in 2006. The tool shows the flow of execution through function calls, showing the path taken through application code, interrupt service routines and context switches.

Similar tools have been applied in the server world, focusing on block

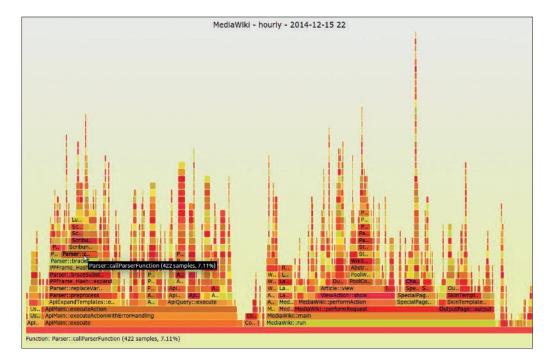
I/O, thread wakeup events or functioncall time, presenting views known as "flame graphs". Because they show time taken in each function stacked on top of the calling code, the graphs tend to resemble a burning fire. The widest flame bases are where the application is spending the bulk of its time.

The server environment tends to use open-source tools, some of which have been incorporated into development environments for embedded systems though suppliers such as Montavista. Other tools, such as Rapitime from Rapita Systems, focus on bulk properties such as worst-case execution time to determine how much variability an application suffers from over hours or days.

#### Overhead imposition

One issue with determining where scheduling and memory-access bottlenecks are affecting an application's performance is that the techniques used to obtain the information themselves can impose an overhead. The most intrusive option is instrumenting the code directly: using a debug build

Below: This flame graph visualises code that's consumed most CPU time



to let function calls themselves update a database of entry and exit timestamps. Adding these calls increases runtime and can inadvertently hide problems because the cache-access patterns change.

Server-based developers tend to use sampling profilers that are less intrusive. These attach to common interrupt service routines and probe each processor's call stack to work out where the application is. There is, naturally, a trade-off between accuracy and performance, making it easy to miss important but short-lived events that may have a knock-on effect on performance.

As embedded developers often have access to hardware trace ports and debug support, they can often avoid the overhead of instrumentation. Although some tools will insert labels into the compiled code to aid with the decoding of the raw trace dump streamed out of the processor, these changes have no impact on actual performance.

The instrumentation situation is being made more complicated by the use of accelerators in both embedded systems and server blades. These can interact with the caches and take over a lot of memory operations but they do not often have their own trace mechanisms. To help deal with the problem, SoC makers are putting performance monitors into their silicon to augment the software trace available from the main processor.

IP suppliers such as UltraSoc propose the use of SoC- or even system-wide debug and trace networks that tap into the various processors and accelerators.

Visualisation tools would bring those pieces of data together into flame graphs and potentially more advanced graphical presentations. As distributed systems morph into systems of systems, such tools will need to evolve to track down the hidden defects that will lead to them suddenly failing to do their job for no apparent reason.



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rtificial intelligence (AI) has kindled the imagination of computer scientists for decades and while the ambition and enthusiasm around AI has tended to clash with the complexity of the task, today's computational power has risen exponentially and the ambition of general AI has been curbed sufficiently to match that power. Computers now learn to recognise patterns in huge, seemingly random datasets - machine learning (ML), and it is no mean feat.

Supervised or unsupervised? Supervised ML is the technique that has been reaping the most successes so far. An ML system is presented with a large dataset and a task.

In the learning phase, the system will be confronted with input, make predictions, and then get feedback through the labels that were preattached to the input - correct or not. If its prediction is false, the ML system will tune its parameters (weights) and make a new prediction. This is done repeatedly, until the parameters are fine-tuned to make more accurate predictions. After the learning phase, the system is ready to mine huge data streams on the lookout for meaningful patterns, a process referred to as inference.

What makes these systems successful is that they require relatively little human effort and pre-processing to fine-tune. With feedback from pre-labelled input, they learn the parameters needed, forming a filter that had to be handcoded previously. But ML systems

# Bringing Alto the edge

Today, Al requires powerful, energyguzzling processors that sit at the heart of the cloud. Bring AI to the sensors at the edge and you could solve that power problem, as **Diederik Verkest** explains

are very power hungry, especially in the learning phase. Even in the inference phase, where the data pass only once through the system, potentially millions of weights have to be taken into account and billions of calculations made. That puts even inference out of reach of where it could be most useful: the fingers and toes of the IoT where the data are sensed and gathered.

To make inference possible at the edge, imec has been developing hardware solutions that drastically cut that energy usage of inference down to the level that fits into autonomous, wireless sensors.

Unsupervised ML requires no human intervention and training. It's the holy grail of ML, and it would allow applications that get customised for specific uses to make decisions on the spot, and not with pre-learned parameters. The techniques and

**Author details** Diederik Verkest is responsible **Machine Learning** programs

algorithms used are loosely inspired on how the human brain learns and functions. But even more than with supervised ML, energy consumption is an issue. Not so much in the cloud, but certainly where customisation is most useful - at the edge, on the sensors.

#### Specialised hardware

As an added challenge, learning and inference cannot be separated.

Customisation is learning, and it has to be included on the sensors. So even more than with supervised ML this will call for specialised hardware. An interesting use case that imec researchers are working on is wearable health technology, where each sensor customises itself to the person who is wearing it.

The dominant hardware platforms involved in supervised machine learning have top-of-line GPUs, consuming up to 200W. Some systems use FPGAs which are on average a tad more power efficient, but which also have a corresponding lower performance. Top of the line in the performance/energy trade-off are a number of ASICs, processors specifically built for deep learning. But even these will still use between 50 and 100W.

No wonder that both machine learning and inference are now done centrally, in the cloud, It's simply not feasible to run a 100W dissipating chip in a mobile phone, let alone in IoT sensors.

However, the IoT sensors are where most of the future data will be



#### ARTIFICIAL INTELLIGENCE PROCESSING AT THE EDGE

captured. In most cases, technical or energy constraints make it impossible to stream all that data to the cloud where the Al resides. In addition, there are also use cases where patterns should be recognised instantaneously, such as with radars that need to detect people or vehicles. There, the time delay of a round-trip to the cloud is simply prohibitive.

So there is a great need to bring machine learning to the edge of the IoT. For supervised learning, that doesn't have to include the learning phase; the parameters can still be learned in the cloud. But surely inference, the smart pattern recognition, should be brought to the sensors.

But what are the energy budgets available at those nodes? Applications in vehicles, for example, can deploy chips that use a maximum of between 10 and 30W. But if you go to the mobile space, you'd have to do inference with 1W. And in IoT, the available budget may even be below 10mW, even going towards 1mW.

Many Al inference systems fetch, over and over again in successive layers, data and weights from memory. Each layer performs multiplications and additions convolutions - and stores the output. The most important priority in designing any low-energy Al chip is therefore minimising both the amount of data that needs to be moved, and the distance it's moved.

Al systems tend to work with 32bit floating-point arithmetic. Minimising the amount of data could be done by lowering that precision, for example

to 8-bit arithmetic. It has been proven that for inference, this can be done with hardly any loss of accuracy. So many 8-bit implementations have been made, but they don't yet bring inference in the energy range of edge computing. A more extreme measure is to bring the precision down to 1-bit, resulting in a so-called binary CNN (convolutional neural network). Unsurprisingly, there is an added accuracy loss compared to 8-bit implementation, but it remains useful for many practical applications.

A second measure is creating an architecture that lowers the energy needed to fetch and store millions of weights and input values over and over again. One solution is to store the learned weights in memory and keep them there, doing inference using a form of analogue in-memory computation. The heart of such an Al processor are thus memory arrays that permanently store the values of the learned weights using analogue non-volatile devices, for example resistive RAM technology.

Each such array represents one layer of the neural network. And in the array, the learned weights are encoded in the individual device conductances.

So how are we then to multiply and add these weights with the input value? By setting the input values as the word line voltages of the ReRAM arrays. Each cell's current will then be the multiplication of the weight and the input value (Ohm's law). And the word line's current will be the summation of the cell currents in that line (Kirchhoff's law). That way, we can effectively implement convolutions



The available computational power has risen onentially to where we are today. And the ambition of general AI has en curbed to match that power: computers now learn to recog atterns in huge, seemingly Diederik Verkest

without having to fetch and move the weights over and over again.

There are challenges to this approach. The variability of the memory chip, for example, will limit the precision with which the weights can be coded. This will especially be an issue with 8-bit precision, but not so much for binary solutions, where STT-MRAM is well suited. There is also the added complexity of integrating an analogue memory in a digital system, requiring, for example, digital to analogue conversions. But the bandwidth gains by not having to move around data far outweigh this added complexity.

#### A pipeline of AI solutions

Scientists at imec are working on a pipeline of solutions that will be demoed in the coming months and

Hardware with non-volatile analogue memories will allow implementing neural network convolutions that use minimal energy, down to the order of milliwatts. They will bring inference to the edge of the IoT, be it with binary or later maybe with a higher precision. This will allow doing smart pattern matching, mining wisdom from huge amounts of sensed data, making the IoT a lot smarter.

The next frontier is hardware for unsupervised ML, hardware that allows for sensors without learned parameters, sensors that can adapt on the fly to individual people and situations. Wearable health sensors, for example, that really and intimately know their wearers.

These will not just make the IoT smarter, but also allow for a more individual experience.



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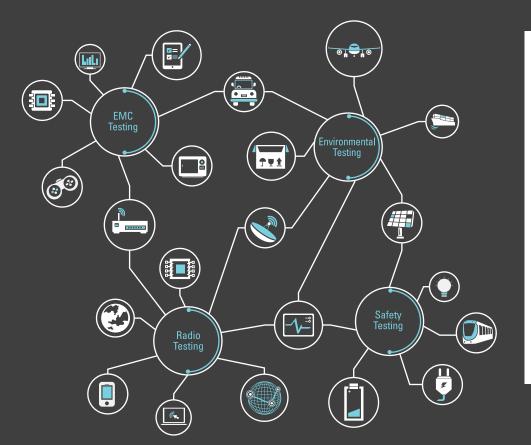






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# From conception to delivery

With various hoops to jump through, the approvals process in the MedTech sector can be challenging, as **Pete Smith** explains

edical technology (MedTech) is one of the most exciting and fast-moving sectors for innovation in the manufacturing market today. Developments in the sector are proving their worth both behind the scenes and in direct contact with patients. From sample prep systems to heart failure monitoring equipment, the technology behind such devices is constantly evolving to deliver streamlined medical processes that make the experience for patients easier.

Whilst the content is exciting,

as with any technology, there are a myriad of hoops through which both the device and developer must jump. In a field where malfunction can mean serious damage to people's health, MedTech is rightfully subject to extensive and rigorous testing.

An Original Equipment
Manufacturer (OEM) is responsible for
guiding its MedTech designs through
this process and, therefore, needs to
be fully aware of the stages involved.
OEMs should also be informed of the
problems that can occur and take
every measure to ensure that these

"All products have to go through two stages of evaluation: pre-compliance testing and then compliance testing."

dangers are carefully controlled.

An effective preventative measure that many OEMs take is to partner with a design to manufacture company that is able to provide electronic engineering and manufacturing services (E2MS). These types of organisation are usually able to offer years of experience in every aspect of the process, from the initial design to the finished product, and help those less experienced to confidently and effectively navigate the testing process.

#### The approvals testing process

All products have to go through two stages of evaluation: pre-compliance testing and then compliance testing.

Pre-compliance testing can be an in-depth review of the product's design at the component level to make sure it complies with key criteria, a functional testing on an early prototype, or both. Both forms of testing ensure that critical parts are correct and key elements of performance act as expected, and identify the ways that the device will be tested for compliance later on.

The aim is to fully inform the design and engineering teams in advance of a final build. Engineers will naturally want to know how the product will perform at the earliest stage possible - ideally before completing a full design. This process lowers the risk to the project's success before final testing takes place by informing the final design and clarifying the changes needed to pass formal compliance testing.

Once pre-compliance testing is complete, formal compliance testing is performed on an official design: an alpha build. The design needs to pass this stage in order to be certified to the appropriate standard and enter the market.

As OEMs and their E2MS partner progress through these stages, they are likely to come up against a number of common obstacles that

#### MEDICAL ELECTRONICS APPROVALS PROCESS

they should be aware of, and prepare for, well in advance.

#### The components

In any device, there is the problem of logistics: how do you integrate all of the electronics inside an enclosure? Cables, power supplies, screens, CPUs and so on, all have to be coordinated in a secure, functional and efficient way, in order to hit the prerequisite standards for device classification.

This process can be further complicated by the need to include certain components, or certain types of components, in order to qualify for a desired classification. The E2MS partner is often expected to provide manufacturing innovation as much as expertise - they need to create devices that provide a unique service, which often means breaking the mould in terms of design.

There is also the issue of timing. OEMs will have strict deadlines to hit in order to successfully deliver the end product onto the market. To prepare for this, both the OEM and any E2MS partner will need to conduct an intensive review of their supply chain. Can they source all the components needed from an individual supplier? Is a change of components going to require contact with a new organisation? Are alternative components being procured beforehand, or is testing being coordinated to dictate intermittent purchases?

These logistics can make or break the delivery of a product. An E2MS will be able to offer exceptional support on the options available to an OEM in terms of developing and procuring the components they need to make their design a reality. An OEM can expect expert support from its partner, which should have the expertise to help them source unique electronic components or even develop their own.

An E2MS partner will also have specialist teams on hand to



collaborate on product development from the design process through testing and onto the build. By considering the manufacturing stage while the product is still being designed, the E2MS provides insight to the OEMs to avoid the use of elements that may prove problematic in the long term.

The tests

Once an OEM is aware of the general standards, a device needs to reach in order to achieve proper certification, they need to clarify how these standards are interpreted. Not all test houses and compliance authorities view them in the same way: an OEM that switches between testers may be unpleasantly surprised to find that an acceptable design to one authority could fail in the eyes of another.

Depending on the field, some devices are going to require more

Above: In a sector where a malfunction can bring serious harm to people's health, MedTech is subject to extensive and rigorous testing

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Solutions for EMEA
at Plexus

compliance tests for a wider range of certifications than others. MedTech devices, for example, are always going to be required to meet standards for electrical safety and EMC/EMI compliance. Today, most medical devices are mandated to comply with risk management and usability standards. Some may even require biocompatibility certification. The full range of certifications available to MedTech devices can be rather intimidating even for an experienced OEM.

As such, it's crucial for an OEM - or its partner - to establish a concrete basis for judgement with the test house. OEMs need to be fully aware of the certifications that the devices will need to meet and then reach out to the relevant authorities to identify exactly what that certification will require. Design files should be shared prior to direct meetings where the tester can give feedback on initial ideas, providing crucial direction on how a device should be developed.

Again, an E2MS partner can provide invaluable support here. It can take on virtually all compliance testing for devices, allowing an OEM to 'divide and conquer' as it chooses in terms of bringing a product to the necessary standard. The extent of this partnership is down to the customer, who will ultimately have to bear full responsibility for the final product.

The extent to which MedTech needs to be tested requires extensive forethought from its designers and manufacturers to make sure that a high-quality device can be delivered on time. The pre-compliance and compliance testing phases make high demands of any OEM, and the logistical planning required is substantial.

By employing a careful, methodical approach – and the expert advice of an experienced E2MS partner– an OEM is capable of delivering valuable devices to market efficiently, but which, in turn, will have a real impact.



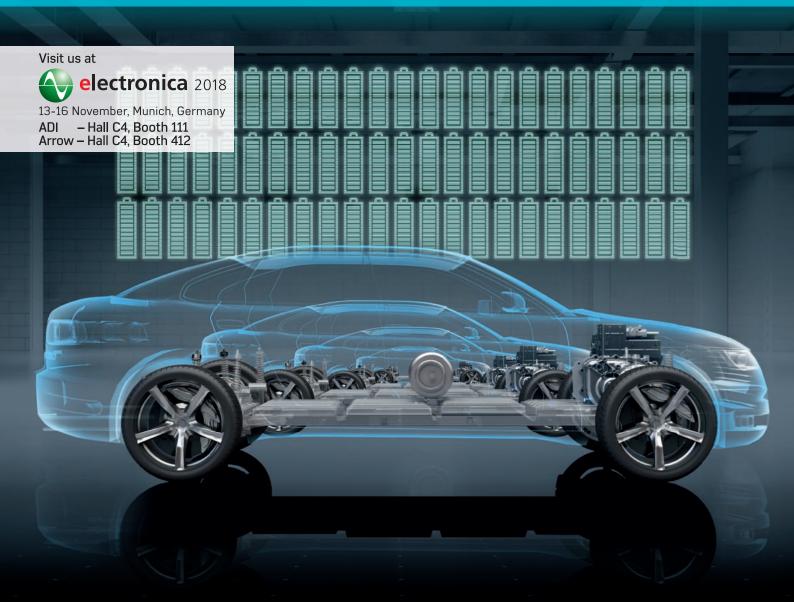


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# ELECTRIFY BATTERY FORMATION AND TEST PRODUCTION





# Safety first and last

According to Arm, without safety there is no future for autonomous driving. By Neil Tyler

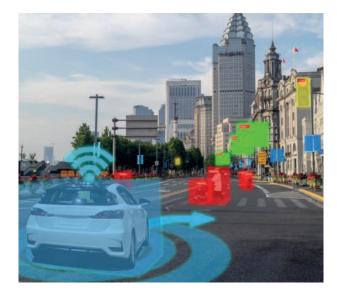
he barriers to self-driving cars are significant, from costs needing to come down to regulations needing to be clarified around certain self-driving car features. Talk of millions of selfdriving cars on the roads within the next few years seems remote, depending on the definition you use, but Lexus, BMW, Apple and Google are all developing, or rumoured to be, automated technology.

Fully-driverless cars are still some way off but partially automated technology has been with us for many

While there is significant investment being made in driverless technology, manufacturers need to tackle a range of ethical and technical issues - chief among them safety.

"Safety is the highest priority for car makers we talk with, for both the obvious technology factors associated with autonomous systems controlling all aspects of driving, but also to ensure that human passengers can trust their automated driver. If consumers don't trust the autonomous systems in their cars are safe, then mass market acceptance of this technology will be slow to happen," says Lakshmi Mandyam, VP Automotive, Embedded & Automotive Line of Business, Arm.

Mandycam makes the point that development costs are increasing exponentially as, "the software complexity and volume for autonomous systems is rising dramatically. To put this into some perspective, it's predicted that a Level 5 vehicle will require a billion lines of code. Compare that to a Boeing 787 Dreamliner, which 'only' requires 14



million lines of code."

When it comes to the safety of autonomous vehicles, however, most of the accidents involving them have been due to human error, so the bigger issue for the industry is what should autonomous vehicles be doing to reduce accidents?

"We are in constant discussion with car makers and our extended automotive ecosystem, which comprises of the top 15 automotive chip makers that license Arm's IP, about progressing toward fullyautonomous driving," says Mandyam. "While we certainly talk about how we can address their performance, power and security requirements, most of the discussions we have tend to focus on safety."

According to Mandyam, autonomous driving is expected to eliminate human error.

"Ninety four per cent of all accidents are a result of driver error and so we expect fully-autonomous driving to significantly reduce the

"If consumers don't trust the autonomous systems in their cars are safe, then mass market acceptance will be slow to happen." Lakshmi Mandyam

number of accidents and fatalities."

Autonomous vehicles will be dependent on sensors to detect what is happening around them and today engineers are defining the right mix of sensors that need to be implemented - but they need to also take into account the costs and computing power required, both are limiting factors.

The other key to vehicle safety will be how the software handles unexpected situations. All self-driving vehicles will have to make many hundreds of decisions every second in order to make adjustments necessary to keep the driver safe.

Vehicles equipped with high levels of autonomy are expected to require 100 times more compute performance by 2024 than is currently the case.

Car makers need to ensure that when it comes to the deployment of autonomous vehicles they are able to provide a safe and efficient compute platform.

"That is why safety cannot be an afterthought or be relegated when it comes to developing autonomousclass SoCs and systems," says

"Unfortunately, the path to level 5 autonomy has tended to be paved with prototypes, often based on power-hungry, expensive data centre CPUs which lack even the most basic functional safety features."

#### **Prioritising safety**

Arm has sought to prioritise safety over many years and that is why, according to Mandyam, the company's IP is now in 65 per cent of the silicon used in ADAS applications.

#### COMMUNICATIONS DESIGN AUTOMOTIVE SAFETY

"Our automotive ecosystem has access to the industry's broadest array of functional safety IP with the latest ISO certifications," she explains.

In fact, Arm's Safety Ready programme encompasses not only existing safe but new and future products which have been through a rigorous functional safety process, including systematic flows and development in support of ISO 26262 and IEC 61508 standards.

Safety Ready is a one-stop shop for software, tools, components, certifications and standards which is intended to simplify and reduce the cost of integrating functional safety. By taking advantage of the programme's offerings, partners and car makers are assured that their SoCs and systems will incorporate the very highest levels of functional safety that are necessary for autonomous applications, says Mandyam.

Ensuring that the company's silicon partners are better supported, Arm is evolving its Safety Ready program and is looking to centralise the company's on-going investment in safety, enabling its silicon partners and the entire automotive supply chain to accelerate individual timelines for bringing safer products to market much faster.

While Arm is looking to integrate the latest certifications and standards in a significant move designed to help the development of autonomous vehicles, it has made available what it says is the first autonomous-class processor with integrated safety, the Cortex-A76AE.

"This processor has been designed for automotive and includes Split-Lock technology, which is available for the first time in application processors and cold be a game changer," says Mandyam.

The Cortex-A76AE is a CPU that has been uniquely designed for automotive and optimised for 7nm process nodes.

The AE stands for "Automotive

Enhanced" and any Arm IP with the AE designator will include specific features addressing the requirements of in-vehicle processing.

"A high level of processing capability is required for autonomous driving, with inherent safety as standard," explains Mandyam, "and the Cortex-A76AE delivers both. It's the industry's first high-performance application processor with Split-Lock capability, combining the processing performance required for autonomous applications and high-integrity safety."

While Split-Lock is certainly not new to the industry, Arm is the first to introduce it to a processor that has been designed specifically for high performance automotive applications such as autonomous drive.

"Split-Lock delivers the



flexibility that's not currently available in previous lock-step CPU implementations; it means that CPU clusters in an a SoC can be configured either in 'split mode' for high performance, where two (or four) independent CPUs in the cluster that can be used for diverse tasks and applications or r 'lock mode' where CPUs are in lock-step, creating one (or two) pairs of locked CPUs in a cluster, for higher safety integrity applications," Mandyam explains.

The CPU clusters can also be configured to operate in a mix of either mode, post silicon production.

Automotive makers can also design their autonomous systems to require

watts and not the kilowatts required for today's prototypes due to the power-efficient computing available in the Cortex-A76AE.

"Lower power also enables a more energy-efficient use of vehicle battery power combined with thermal efficiency to aid the packaging of compute capability while extending the range of vehicles for a lower total cost of driving," according to Mandyam.

Arm is also introducing new Automotive Enhanced system IP for designing a comprehensive autonomous-class SoC.

The new CoreLink GIC-600AE, CoreLink MMU-600AE and CoreLink CMN-600AE will provide critical elements such as high-performance interrupt management, extended virtualization and memory management, and connectivity to multiple CPU clusters to scale performance in safe multicore systems.

"These products have been designed to enable high-performance systems, targeting ASIL-B to ASIL-D safety integrity, and support the Split-Lock and systematic capabilities for functional safety designed into the Cortex-A76AE."

The Cortex-A76AE is the first in a roadmap of "Automotive Enhanced" processors which will deliver the fullest functional safety capable IP portfolio in the industry. The new roadmap includes "Helios-AE" and "Hercules-AE", all optimised for 7nm. More details will be available, as these products are launched.

According to Mandyam, "Arm and its developer ecosystem are simplifying and reducing costs across all layers of automotive software stacks and providing tools on a common architecture.

"Our aim has to be to ensure that safety is not an afterthought and to help car makers earn the consumer trust required for the mass deployment of safe and fullyautonomous vehicles."

#### 8GHz solid-state RF PXI switches

Wide-ranging family of 8GHz solid-state RF PXI switches launched by **Pickering Interfaces** 

Modular format for easy system integration

Pickering Interfaces, a leading provider of modular signal switching and simulation products for electronic test and verification, today launched a 13-model family of 8GHz solid-state RF PXI switches, including SPDT, SP4T, SP6T, SP8T, SP16T and 4x4 Matrix devices. Pickering Interfaces' series 40-88xA high-performance switch family now covers 10MHz to 8GHz in the modular PXI format for easy system integration.

Targeting the telecoms and semiconductor test industries and compatible with a wide range of platforms including PXI, PXIe Hybrid and Pickering USB/LXI chassis, all the new units feature automatic termination of unused switch channels, up to +36dBm input power handling and excellent RF performance characteristics. Single, dual, quad, hex and octal versions are available on some family members.

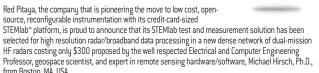
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**Dual-mission HF radars** 

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#### New 19" Mini-Rack Enclosures

#### **METCASE Launches New 19" Mini-Rack**

METCASE has created a new mini-rack version of its advanced TECHNOMET table-top instrument enclosures which is designed for mounting standard 19" subracks, chassis and front panels.

These elegant and modern enclosures are available in three standard sizes: 3U, 4U and 6U, all 400 mm deep. Standard 19" panel mounts are included in the front bezels. The cases are ventilated and include chassis support rails inside. All case panels include earth connections. ABS side handles and non-slip feet are also included.

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#### OMC's new high brightness purple LED brings greater flexibility for designers

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OMC, the pioneer in optoelectronics design & manufacture, has launched a new high brightness purple surface-mount LED lamp featuring the company's proprietary Active Diffuser Technology™, which produces a far richer and more efficient

output than traditional single-wavelength devices. The vibrant output and ease of driving of the new purple LED SMD lamp makes it ideal for applications such as backlighting, mood-lighting, displays and status indication on items such as front panels and keypads, as well as signalling and industrial electronics. Designated LPRM3268X3, this new SMD lamp requires very low current, has a compact footprint of only 3.2mm by 2.8mm, and a depth of 1.9mm, with the industry-standard PLCC package.

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#### PicoCore MX6SX

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#### SpaceX Hyperloop challenge

#### Nicomatic-sponsored WARR Hyperloop team wins SpaceX Hyperloop challenge by going 50% faster

Lightweight, compact and rugged connectors contribute to University of Munich team's success

Nicomatic, the leading manufacturer of high-performance interconnect solutions, is delighted to announce that the WARR Hyperloop Team from the Technische Universität of Munich (TUM) has won the 2018 SpaceX Hyperloop Pod competition by going almost 50% faster than in 2017, achieving a final speed of 467 km/h. Nicomatic is the team's only connector sponsor and Nicomatic's micro-connectors contributed to this success by delivering reliable performance under challenging race conditions, while minimizing space and weight.

Hyperloop is a new transportation concept proposed by Elon Musk, founder of Tesla and SpaceX in 2013, in which a high speed train travels in a near-vacuum tube. The reduced air resistance in the tube allows the pod to reach speeds of more than 1000 km/h.

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#### Ultra-Low Power sensAl Stack

#### Lattice Expands Ultra-Low Power sensAl Stack with Optimized Solutions for Always-On, On-Device Al

CNN accuracy with flexible milliwatt FPGA solutions; New reference designs for human presence and hand gesture recognition with scalable performance/power

Lattice Semiconductor Corporation (NASDAQ: LSCC) today unveiled expanded features of the company's popular Lattice sensAl™ stack designed to speed time-to-market for developers of flexible machine learning inferencing in consumer and industrial IoT applications. Building on the ultra-low power (1 mW-1 W) focus of the sensAl stack, Lattice is releasing new IP cores, reference designs, demos and hardware development kits that provide scalable performance and power for always-on, on-device artificial intelligence (AI) applications.

"Flexible, low-power, always-on, on-device Al is increasingly a requirement in edge devices that are battery operated or have thermal constraints. The new features of the sensAl stack are optimized to address this challenge, delivering improved accuracy, scalable performance, and ease-of-use, while still consuming only a few milliwatts of power"

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